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By: John P. [Signature]

Date: 3/15/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Hans-Jürgen Hacke et al.
Applic. No. : 09/761,594
Filed : January 16, 2001
Title : Semiconductor Device in Chip Format and Method for
Producing It

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

United States Patent No. 4,922,321 (Arai et al.), dated May 1, 1990;

United States Patent No. 5,074,947 (Estes et al.), dated December 24, 1991;

United States Patent No. 5,477,087 (Kawakita et al.), dated December 19, 1995;

European Patent Application EP 0 734 059 A2 (Akagawa et al.), dated September 25, 1996;

Japanese Patent Abstract JP 05 062 981 (Takashi), dated March 12, 1993;

Japanese Patent Abstract JP 06 232 134 (Shigeyuki), dated August 19, 1994;

[Handwritten mark]

International Publication WO 96/22620 (Pedersen et al.), dated July 25, 1996;

Shinji Baba et al.: "Molded Chip Scale Package for High Pin Count", 1996 Electronic Components and Technology Conference, pp. 1251-1257, XP 000684987;

"Solder Plated Resin Ball", IBM Technical Disclosure Bulletin, Vol. 38 (1995) May, No. 5, pp. 463-464.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,



For Applicants

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